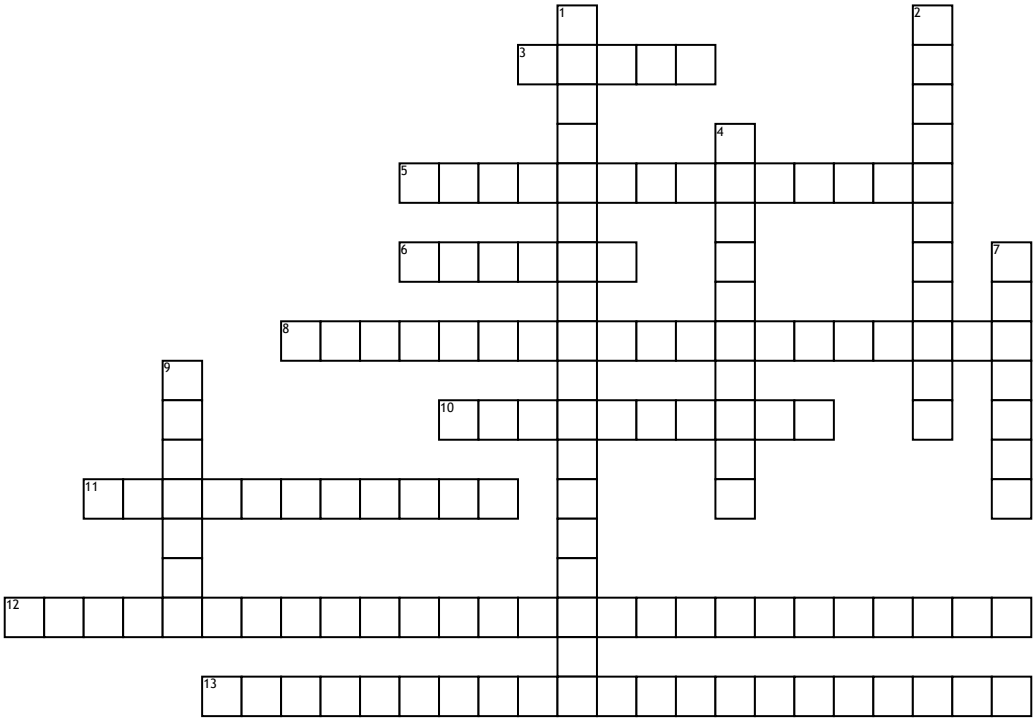
Name: _____ Date: _____

Von Neumann Architecture



Across

3. Part of the CPU cycle that retrieves data from memory.

5. Holds the memory address of the next instruction to be fetched from primary memory

6. Part of the CPU cycle that Interprets an instruction.

8. CPU Component that performs arithmetic and logic calculations.

10. Carries memory addresses from the processor to other components. e.g. primary memory

11. Holds the data being processed and the results of processing

12. Holds the instruction that is currently being decoded and executed

13. holds the address of the current instruction that is to be fetched from memory, or the address in memory to which data is to be transferred

Down

1. Holds the contents found at the address held in the MAR, or data which is to be transferred to primary memory

2. CPU Component that manages instructions.

4. Carries control signals from the processor to other components.

7. Carries data between the processor and other components.

9. Part of the CPU cycle that Carries out an instruction.

Word Bank

Address bus
program counter
memory address register
execute
accumulator
arithmetic logic unit
decode
fetch
memory data register
control unit
current instruction register
Data bus
Control bus