Name: _____ Date: _____

Logic Gates

E N B W V L U I N Z R D I N P U T
I N V E R T E R A M W O D D B O U
S E T A G M T M N D Q B B D D N A
B T O N W G T C D L J I B H J D N
D N Y U J W O I C Y N N D X C V R
Q L D W H L O B M Y S A Q M E Q O
E L B A T H T U R T Q R R D E X N
C I G O L X C Y P M B Y U O R Z W
Y S M C O M B I N A T I O N A L V
U D J T M J C O G M V H T B D R J
D B Y T K I S C I N O R T C E L E
D D M V R V W M E G R W A Y U J E
F L D C E X P R E S S I O N E O B
Z U U O U T P U T Y U T Z A X E H
K I I E S V U R B F W C K B M R A
T Z X X Z S D J C V F Y K R H W V
D U T Z O V B D I G I T A L X O F

combinational
inverter
output
logic
not
truth table
digital
binary
nand
or
electronics
circuit
input
nor
expression
symbol
gates
and